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EXAMINER	
KALAM, ABUL	

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2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,838	UEDA, NAOHIRO	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. In the amendments filed on January 24, 2007, claims 1-10, 17 and 18 are were amended. Thereby, claims 1-10, 17 and 18 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 2 and 4-6** are rejected under 35 U.S.C. 102(b) as being anticipated by **Rodriguez et al. (US 5,821,160, previously cited, hereinafter, Rodriguez)**.

With respect to **claim 1, Rodriguez** teaches a semiconductor apparatus **(FIG. 7)** comprising:

a semiconductor substrate **(12, FIG. 7)**;

an electrode pad **("bonding pads")** including a metal layer **(54)** and formed over the semiconductor substrate **(col. 6: lns. 48-53)**;

a MOS transistor **(NMOS)** formed over the semiconductor substrate **(col. 3: lns. 59-61, col. 4: lns. 35-52)**; and

an analog circuit formed in a region under the electrode pad **(54)**, said analog circuit formed over the semiconductor substrate and comprising a resistive element **(42)** including a semiconductor material **("polysilicon") (col. 5: lns. 28-29, 34-36)**.

Regarding the limitation "analog circuit," applicant claims that the analog circuit is comprised of a resistive element including a semiconductor material. Therefore, the integrated circuit taught by **Rodriguez**, which comprises a resistive element **(42, col. 5: lns. 28-29)**, can also be considered an analog circuit.

With respect to **claim 2, Rodriguez** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive element **(42)** includes a specific material made of polysilicon **(col. 3: lns. 59-61, col. 4: lns. 35-52)**.

With respect to **claim 4, Rodriguez** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the MOS transistor **(NMOS)** comprises a gate electrode **(21; FIG. 2)** including a specific material **("polysilicon")** of the resistive element **(42) (col. 3: lns. 59-61, col. 4: lns. 13-23)**.

With respect to **claim 5, Rodriguez** teaches the semiconductor apparatus as set forth in claim 1 above, further comprising:

an insulating film **(32)** formed on the semiconductor substrate **(12)** in a region in a vicinity of the electrode pad **(54) (FIG. 7; col. 4: lns. 42-47)**; and

a fuse element **(36)** formed on the insulating film **(32) (col. 4, lns. 53-67)**.

With respect to **claim 6, Rodriguez** teaches the semiconductor apparatus as set forth in claims 1 and 5 above, wherein the fuse element **(36)** includes the specific material of the resistive element **("polysilicon") (col. 4, lns. 53-67)**.

3. **Claims 1-4 and 17** are rejected under 35 U.S.C. 102(b) as being anticipated by **Takasu et al. (US 6,369,409, previously cited, hereinafter, Takasu)**.

With respect to **claim 1, Takasu** teaches a semiconductor apparatus **(FIG. 12A-12F)** comprising:

a semiconductor substrate **(801; FIG. 12A, col. 8: lns. 9-10)**;

an electrode pad **("bonding pads")** including a metal layer **(814; FIG. 12F)** and formed over the semiconductor substrate **(col. 9: lns. 43-56)**;

a MOS transistor **("N-type transistor")** formed over the semiconductor substrate **(col. 9: lns. 23-28)**; and

an analog circuit formed in a region under the electrode pad, said analog circuit formed over the semiconductor substrate and comprising a resistive element **(807; FIG. 12D)** including a semiconductor material **("polysilicon") (col. 9: lns. 28-67)**.

Regarding the limitation "analog circuit," applicant claims that the analog circuit is comprised of a resistive element including a semiconductor material. Therefore, the circuit taught by **Takasu**, which comprises a resistive element **(807)**, can also be considered an analog circuit.

With respect to **claim 2, Takasu** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive element **(807)** includes a specific material made of polysilicon **(col. 9: lns. 28-30)**.

With respect to **claim 3, Takasu** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive element includes a plurality of resistors **(807; FIG. 2D) (col. 9: lns. 28-33, 56-58)**.

With respect to **claim 4, Takasu** teaches a semiconductor apparatus as set forth in claim 1 above, wherein the MOS transistor **("N-type transistor")** comprises a gate

electrode **(806; FIG. 12D)** including a specific material **("polysilicon")** of the resistive element **(807; FIG. 12D) (col. 9: lns. 10-33)**.

With respect to **claim 17, Takasu** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive element includes a plurality of doped semiconductor material resistors **(807; FIG. 12D) (col. 9: lns. 10-33)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Rodriguez ('160)** as applied to claim 5 above, and further in view of **Matsuzaki et al. (US 2002/0063262, previously cited, hereinafter, Matsuzaki)**.

With respect to **claim 7, Rodriguez** teaches all the limitations of the claim, as set forth above in claim 1, with the exception of disclosing:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad.

However, **Matsuzaki** teaches a semiconductor apparatus **(FIG. 3)** wherein a rerouting layer **(148)** is formed in a region above a fuse element **(142; pg. 5: [0093])**;

and an external connection terminal **(150)** is formed on the rerouting layer in a region different from a formation region of the electrode pad **(143) (pg. 4: [0080]-[0081])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of **Rodriguez** to include a rerouting layer and external connection terminal on the rerouting layer, as taught by **Matsuzaki**, for the disclosed intended purpose of connecting the semiconductor apparatus to an electrode of another chip, thereby forming a multi-chip apparatus **(pg. 4: [0082])**.

5. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rodriguez ('160)** as applied to claim 5 above, and further in view of **Tsuchida (US 6,232,823, previously cited)**.

With respect to **claim 8, Rodriguez** teaches the semiconductor apparatus as set forth in claim 5 above, with the exception of disclosing:

wherein the analog circuit comprises a voltage setting circuit, the resistive element comprises at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

However, **Tsuchida** teaches voltage setting circuit **(fig. 1)**, in which a resistive element comprises at least two resistors (**22, 23, 24, 25, 26**) for producing a split voltage based on an input source power voltage (**21**), and the voltage setting circuit changes the split voltage according to a condition of the fuse element (**27, 28, 29, 30**) **(col. 7: lns. 7-64)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor apparatus of **Rodriguez** to include a voltage setting circuit, as taught by **Tsuchida**, for the disclosed intended purpose of providing a voltage setting circuit, in which the number of choices in the output voltage is increased while suppressing the increase of an area occupied by resistors **(col. 2, lns. 24-27)**.

With respect to **claim 9, Rodriguez** teaches the semiconductor apparatus as set forth in claim 1 above, and **Tsuchida** teaches **(fig. 6)** wherein the resistive element comprises at least two resistors (**22, 23, 24, 25, 26**) for producing a split voltage **(col. 11: lns. 51-55; col. 7: 45-64)** based on an input source power voltage **(53)**, the analog circuit comprises a reference voltage generator **(51)** for generating a reference voltage **(col. 11: lns. 61-63)** and a voltage detector including a comparator **(52)** for performing a comparison of the split voltage with the reference voltage **(col. 11: lns. 50-67; col. 12, lns. 1-33)**. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of **Rodriguez** with the teachings **Tsuchida,** for the reasons stated above in claim 8.

With respect to **claim 10, Rodriguez** and **Tsuchida** teach the semiconductor apparatus as set forth in claim 9 above, and **Tsuchida** also teaches **(fig. 6)** wherein the apparatus further comprises an output driver **(54)** for controlling an output voltage **(55)** based on an input voltage **(53)**, and the comparator **(52)** of the voltage detector outputs a gate control voltage **("operation voltage")** as a result of the comparison for controlling the output driver **(54)** to control the output voltage **(col. 11, lns. 61-67; col.**

12, lns. 1-5). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of **Rodriguez** with the teachings **Tsuchida,** for the reasons stated above in claim 8.

6. **Claims 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Rodriguez ('160)** as applied to claim 5 above, and further in view of **Kohda et al. (US 5,107,313, previously cited, hereinafter, Kohda)**.

With respect to **claim 18, Rodriguez** teaches all the limitations of the claim, as set forth above in claim 4, with the exception of explicitly disclosing wherein said gate electrode has lengthwise ends which are bent in an upward direction over an insulating film.

However, **Khoda** teaches a semiconductor apparatus wherein the gate electrode **(4b)** has lengthwise ends which are bent in an upward direction over an insulating film **(2) (FIG. 10; col. 6, lns. 6-12)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of **Rodriguez** to form the gate electrode with lengthwise ends bent in upward direction over an insulating film, as taught by **Khoda**, for the disclosed intended purpose of reducing the horizontal spacing between the gates, which thereby reduces the cell area and leads to a higher cell density of memory devices **(col. 6: lns. 21-24)**.

Response to Arguments

7. Applicant's arguments with respect to claim 1-10, 17 and 18, filed January 24, 2007 have been fully considered but are not persuasive.

Applicant argues that Rodriguez does not illustrate the "bond pads" in any of the figures. This argument is not persuasive because, Rodriguez clearly states in col. 6, lines 48-55, that the bond pads (electrode pad) are formed from metal **54** which is clearly formed over the semiconductor substrate **12**, as shown in Fig. 7. Thus it is implicit that the bond pads (electrode pad) are formed over the substrate.

Applicant argues that the figures in Rodriguez do not illustrate whether there is an "analog circuit" containing polysilicon layer 42 beneath the "bond pad areas" of the metal layer 54. This argument is not persuasive because applicant defines the analog circuit as a resistive element including a semiconductor material **(claim 1, lns. 6-8)**. Rodriguez clearly describes polysilicon layer **42** as a resistor element **(col. 5: lns. 28-29)**, which is coupled to transistor electrodes **(col. 5: lns. 31-34)**. Furthermore, the analog circuit **(polysilicon resistor element 42)** is formed in a region under the electrode pad **(bond pads made of metal 54)**, as shown in Fig. 7. As stated above, it is implicit that the bond pads are formed over the substrate **12** and the polysilicon resistor **42**, because the bond pads are formed from the metal regions **54** by etching the oxides over the metal regions **(col. 6: lns. 48-55)**. Furthermore, note that although the electrode pad ("bond pads") is not illustrated in the figures, Rodriguez clearly discloses and teaches the limitation of an electrode pad by his description of "bond pads" being formed of metal regions **58 (col. 6: lns. 48-55)**.

Applicant argues that Takasu does not illustrate "bond pads" in any of the figures and furthermore, the figures do not illustrate whether there is "analog circuit" beneath the "bond pads." Again, applicant seems to be arguing that because limitations are not shown in the figures, the reference does not teach such limitations. This argument is not persuasive because, Takasu clearly discloses that protective film **815** is partially removed to form a bonding pad **(col. 9: lns. 54-56)**. Thus, it is implicit that part of aluminum layer **814**, which is formed above the substrate **801** and the analog circuit **(resistors 807)**, comprises an electrode pad **("bonding pad") (FIGs. 12A-12F, col. 9: lns. 43-56)**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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